Area-Efficient Fault Tolerant Design for Finite State Machines

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Abstract—The finite state machine (FSM) controls the operation of the entire system. Therefore, if the errors occur in the FSM, it causes serious problem of the system. The fault tolerant state machine is proposed to deal with the errors in the FSM. In this paper, we propose a selective fault-tolerant finite state machine that increases fault-tolerance by applying the fault-tolerant circuit selectively according to the importance of state. The proposed SFT-FSM is 39% smaller when the redundancy factor N is 9, compared to the FSM with NMR technique.

Keywords—digital circuit control, FSM, fault-tolerant, time-redundancy, selective fault-tolerant

I. INTRODUCTION

Finite State Machines (FSMs) are used to control the operation of a device by defining a finite number of states that operate digital circuits and determining transitions between the states [1]. As it controls the behavior of the entire circuit system, it can cause fatal problems for the whole system when an error occurs. If the state changes due to an error in the FSM from an uncontrollable factor, a Single Event Upset (SEU) occurs, in which the circuit operates differently from the designer's intention [2]. Therefore, a fault tolerant FSM has been developed to prevent malfunction from SEUs [3].

In this paper, we propose an FSM with a selective fault tolerance technique according to the importance of the state by using time in replication. The proposed selective fault tolerant FSM (SFT-FSM) determines the importance of the current state. Further, when it is determined as critical, the fault-tolerant circuit is repeatedly operated by the redundancy factor N, improving the reliability of the critical state.

II. FAULT TOLERANT TECHNIQUE

Among the fault tolerant technique, triple modular redundancy (TMR) is the representative hardware redundancy technique. Therefore, we designed the N modular redundancy FSM (NMR-FSM) for fault tolerant and the proposed selective fault tolerant FSM (SFT-FSM).

A. N-Modular Redundant FSM (NMR-FSM) Operantion

N-Modular Redundancy (NMR) operates by N-plicating and working in parallel to the error-sensitive part of the circuit
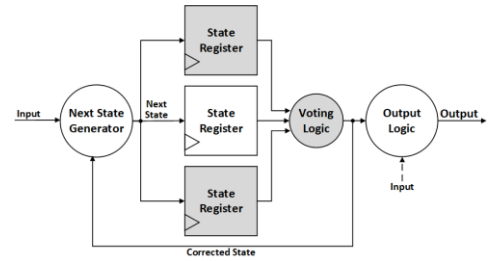

Fig. 1. NMR-FSM structure when the redundancy factor N is 3

for fault tolerance. It then determines the final output through a majority vote based on the output of each circuit [5]. Fig. 1 shows an FSM with Triple Modular Redundancy (TMR) applied to the state register, assuming that an error occurs in the sequential circuit [4].

NMR [5] can correct up to n errors, where n is $(N–1)/2$. The probability of error in NMR-FSM, $P_{\mathrm{NMR}}(e)$, is the same as (1), where p is the probability of error in one flip-flop, e is the number of errors, and s is the number of bits in the state register.

$$P_{\mathrm{NMR}}(e) = 1 - \left(\sum_{e=0}^{n} {}_N C_e p^e (1-p)^{(N-e)} \right)^s , \qquad (1)$$

B. Selective Fault Tolerant FSM (SFT-FSM) Operation

The proposed SFT-FSM enhances the reliability of the entire circuit by repeating the fault tolerant circuit by the redundancy factor N according to the importance of each state. The circuit structure of an FSM with SFT-FSM is shown in fig. 2. When an FSM receives an input, the next state is determined by the next state generator considering the current state and the input. The next state is stored in the state register and then outputted to the current state in the next cycle. It is determined whether the outputted current state is critical or not in determining the operation of the fault-tolerant circuit. If the state is not critical, the current state is inputted into the next state generator, and the current state is stored in *Prev_Reg*. If the outputted state is a critical state, the selective fault tolerant circuit is repeated by the redundancy factor N. In the first iteration, the current state, which is the object of comparison with the output of the state register for the next iterations, is stored in *Next_Reg*. The current state input in the next state
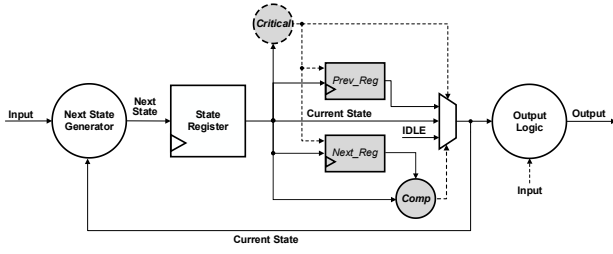
Fig. 2. The proposed SFT-FSM structure

function contains the value stored in *Prev_Reg*. From the second to $N-1$ repetition, compare the current state output from the state register with the value stored in *Next_Reg*. If the two states match, the value stored in *Prev_Reg* is outputted, otherwise, the *IDLE* state is outputted to initialize the circuit. In the *N*th repetition, the current state output from the state register is compared with the value stored in *Next_Reg*. If the two values are the same, the current state is outputted; otherwise, the *IDLE* state is outputted to initialize the circuit.

The probability that an error occurs because SFT-FSM outputs the incorrect state as the final output, $P_{\text{SFT-FSM}}(e)$, is shown in (2), where p is the probability that an error occurs in one flip-flop, e is the number of errors, s is the number of bits in the state register, and N is the number of repetitions. The larger the N, the lower the probability of error occurrence.

$$P_{\text{SFT-FSTM}}(e) = \sum_{e=1}^{s} {}_{s}C_e (p^N)^e (1-p)^{N(s-e)} \ . \tag{2}$$

III. Experimental Results

To compare the reliability of the proposed SFT-FSM and NMR-FSM, the error probability is shown in Figure 4 according to the reliability. One state is composed of 10 bits, and it is assumed that the redundancy factor N is 5, 7, or 9. Fig. 3 shows that the proposed SFT-FSM has better error detection performance than the NMR-FSM for the same redundancy factor.

To compare the area and delay time of NMR-FSM and SFT-FSM, we set one state that is composed of 10 bits and the maximum number of representable states being 1,024. The number of critical states is 102 which is 10% of the total number of states. Table I shows the result and delay time of NMR-FSM and the proposed SFT-FSM synthesized at 200 MHz operating frequency using CMOS 180 nm process. The proposed SFT-FSM requires N cycles of delay time only in critical states and the same cycle delay time of 1 as in NMR-FSM in non-critical states. It can be seen that the product of the area and delay time of the SFT-FSM is smaller by about 39% compared with the NMR-FSM when the redundancy factor is 9.

IV. Conclusion

In this study, we proposed the SFT-FSM that can be applied to a system that requires high stability. The proposed SFT-FSM has higher reliability than NMR-FSM. Additionally, the larger the redundancy factor N, the more advantageous in

TABLE I.   Synthesis Result of NMR-FSM and SFT-FSM

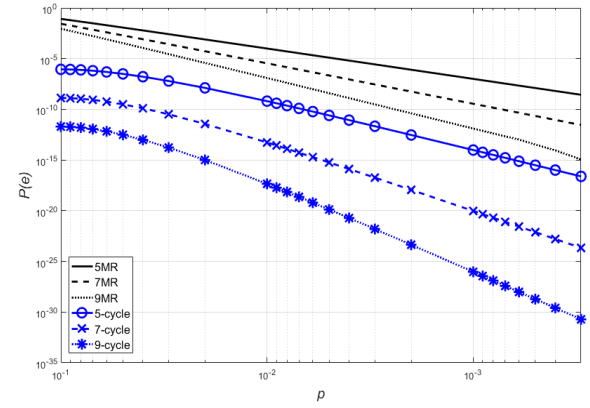| N	FTFSM	Gate Count	Average Latency	Area × Time
5	NMR	739.7	1.0	739.7
	S-FTFSM	501.1	1.4	700.7
7	NMR	970.6	1.0	970.6
	S-FTFSM	516.7	1.6	821.5
9	NMR	1,468.4	1.0	1,468.4
	S-FTFSM	506.2	1.8	906.1

Fig. 3. The error probability of NMR-FSM and SFT-FSM

terms of area and delay time the SFT-FSM is compared with the NMR-FSM. This indicates that SFT-FSM can be applied to the FSM of a system that requires high reliability, mitigating the error of the FSM and enhancing the reliability and stability of the whole system.

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